<table>
<tr><td>25</td><td>RO</td><td>Host Regulator Voltage Stable
This status is added from Version 4.10 and is used to check whether host regulator voltage is stable for switching signal voltage of UHS-I mode.

<table><tr><td>1</td><td>Host Regulator Voltage is stable</td></tr><tr><td>0</td><td>Host Regulator Voltage is not stable</td></tr></table>
Support of this function is checked by reading this status after that Software Reset For All in the Software Reset register is cleared by the Host Controller in initialization. Setting of this status means that the Host Controller supports this function.

This status may be related to 1.8V Signaling Enable in the Host Control 2 register. Changing 1.8V Signaling Enable causes unstable of host regulator voltage for I/O cell. Then once this status is set to 0 and retrieved to 1 when host regulator voltage is stable again. When executing power cycle, Host Driver also executes Software Reset For All and it clears 1.8V Signaling Enable to go back signal voltage to 3.3V.

If this status is not supported, Host Driver should take more than 5ms for stable time of host voltage regulator from changing 1.8V Signaling Enable. Specific Host Driver may use a specific time, which is provided by Host System, instead of using 5ms.</td></tr>
<tr><td>24</td><td>RO</td><td>CMD Line Signal Level (SD Mode only)
This status is used to check the CMD line level to recover from errors, and for debugging.</td></tr>
<tr><td>23-20</td><td>RO</td><td>DAT[3:0] Line Signal Level (SD Mode only)
This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0].

<table><tr><td>D23</td><td>DAT[3]</td></tr><tr><td>D22</td><td>DAT[2]</td></tr><tr><td>D21</td><td>DAT[1]</td></tr><tr><td>D20</td><td>DAT[0]</td></tr></table></td></tr>
<tr><td>19</td><td>RO</td><td>Write Protect Switch Pin Level
The Write Protect Switch is supported for memory and combo cards.
This bit reflects the SDWP# pin.

<table><tr><td>1</td><td>Write enabled (SDWP#=1)</td></tr><tr><td>0</td><td>Write protected (SDWP#=0)</td></tr></table></td></tr>
<tr><td>18</td><td>RO</td><td>Card Detect Pin Level
This bit reflects the inverse value of the SDCD# pin. Debouncing is not performed on this bit. This bit may be valid when Card State Stable is set to 1, but it is not guaranteed because of propagation delay. Use of this bit is limited to testing since it must be debounced by software.

<table><tr><td>1</td><td>Card present (SDCD#=0)</td></tr><tr><td>0</td><td>No card present (SDCD#=1)</td></tr></table></td></tr>
</table>